
Lab Module 2: CMOS Inverter Design and Static Characteristics Analysis

Discipline: Digital VLSI Design

Module Title: CMOS Inverter Design and Static Characteristics Analysis

Duration: 3 Hours (or two 90-minute sessions)

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1. Aim:

The primary aim of this lab is to design and simulate the most fundamental CMOS gate, the inverter, using a circuit simulation tool. Through this process, students will systematically analyze its static behavior, extract critical Voltage Transfer Characteristic (VTC) parameters, calculate noise margins, and investigate the profound impact of transistor Width-to-Length (W/L) ratios on these characteristics.

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2. Theory:

The CMOS (Complementary Metal-Oxide-Semiconductor) inverter is the cornerstone of all digital logic circuits. It consists of an n-type MOSFET (nMOS) and a p-type MOSFET (pMOS) connected in series between VDD (power supply) and GND (ground). The gates of both transistors are tied together to form the input (Vin), and their drains are connected to form the output (Vout).

- **nMOS Transistor:** Acts as a pull-down device. When Vin is high, the nMOSFET turns ON, creating a low-resistance path between Vout and GND, pulling Vout to logic '0'. When Vin is low, the nMOSFET turns OFF, creating a high-resistance path.
- **pMOS Transistor:** Acts as a pull-up device. When Vin is low, the pMOSFET turns ON, creating a low-resistance path between Vout and VDD, pulling Vout to logic '1'. When Vin is high, the pMOSFET turns OFF, creating a high-resistance path.

In a well-designed CMOS inverter, one transistor is ON while the other is OFF, which ideally leads to negligible static power consumption.

Voltage Transfer Characteristic (VTC): The VTC is a plot of Vout versus Vin for a given inverter. It is a fundamental tool for analyzing the static behavior of the inverter. Key parameters extracted from the VTC are:

- **VOH (Output High Voltage):** The maximum output voltage (ideally VDD) when the input is a valid logic low.
- **VOL (Output Low Voltage):** The minimum output voltage (ideally 0V) when the input is a valid logic high.
- **VIL (Input Low Voltage):** The maximum input voltage that is still reliably interpreted as a logic low. This is the point on the VTC where the slope (dVout/dVin) is -1.
- **VIH (Input High Voltage):** The minimum input voltage that is still reliably interpreted as a logic high. This is the point on the VTC where the slope (dVout/dVin) is -1.

- **Vth (Switching Threshold Voltage):** Also known as Vinv or Vtrip, it is the input voltage at which Vout = Vin. It signifies the point where the inverter transitions its output state. For a balanced inverter, Vth is ideally VDD/2.

Noise Margins: These quantify the circuit's ability to tolerate noise.

- **NML (Noise Margin Low):** Represents the maximum noise voltage that can be tolerated on a logic '0' input without causing the output to incorrectly switch. NML = VIL - VOL.
- NMH (Noise Margin High): Represents the maximum noise voltage that can be tolerated on a logic '1' input without causing the output to incorrectly switch. NMH = VOH - VIH.
  For robust operation, NML and NMH should be as large and as equal as possible.

Impact of W/L Ratio: The Width-to-Length (W/L) ratio of a MOSFET directly affects its current driving capability. A larger W/L means a stronger transistor. Due to differences in electron and hole mobilities (electrons typically move faster than holes), a pMOSFET needs to be wider (larger W/L) than an nMOSFET to provide equivalent current drive. Typically, the (W/L)pMOS / (W/L)nMOS ratio is around 2-3 to achieve a symmetrical VTC with Vth near VDD/2 and balanced noise margins. Varying these ratios will shift the VTC and impact noise margins significantly.

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3. Pre-lab Questions:

Students must answer these questions before beginning the lab session.

1. Draw the circuit schematic of a basic CMOS inverter, clearly labeling all terminals of the nMOS and pMOS transistors, input, output, VDD, and GND.
2. Explain why the bulk terminal of the pMOSFET is connected to VDD and the bulk terminal of the nMOSFET is connected to GND. What is the phenomenon that these connections help prevent?
3. What is the significance of the Voltage Transfer Characteristic (VTC) of an inverter? Sketch an ideal VTC and a typical real VTC.
4. Define VIL, VIH, VOH, and VOL from the VTC perspective.
5. Derive the formulas for NML and NMH. Explain what each noise margin signifies in terms of circuit robustness.
6. Why is the W/L ratio of the pMOSFET typically chosen to be larger than that of the nMOSFET in a CMOS inverter?
7. If the nMOSFET in an inverter is made significantly stronger (larger W/L) than the pMOSFET, how would you expect the VTC to shift? Specifically, how would Vth be affected?

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4. Procedure:

Part A: Basic CMOS Inverter Schematic Capture and Initial VTC Analysis

1. **Launch Circuit Simulation Software:** Open your designated circuit simulation environment (e.g., Cadence Virtuoso, LTSpice, HSPICE, etc.).
2. **Create a New Library/Project:** Create a new design library or project for this lab.
3. **Schematic Entry:**
    - Place an nMOSFET and a pMOSFET from the provided technology library. (Note: Use typical technology parameters if not specified, e.g., 180nm, 90nm, etc., and a nominal VDD, e.g., 1.8V, 1.0V).
    - Set initial W/L ratios:
        - nMOSFET: W = 1 µm, L = 0.18 µm (or your technology's minimum length)
        - pMOSFET: W = 2 µm, L = 0.18 µm (or your technology's minimum length)
        - *(Instructor Note: Adjust these W/L values based on your specific technology library to achieve reasonable initial performance.)*
    - Connect the gates together as the input (label as Vin).
    - Connect the drains together as the output (label as Vout).
    - Connect the pMOSFET source to VDD (e.g., 1.8V DC voltage source).
    - Connect the nMOSFET source to GND (0V).
    - Connect the pMOSFET bulk to VDD.
    - Connect the nMOSFET bulk to GND.
    - Place input and output pins/labels.
4. **DC Analysis Setup:**
    - Configure a DC voltage source for Vin.
    - Set up a DC Sweep simulation:
        - Sweep Variable: Vin
        - Start Value: 0 V
        - Stop Value: VDD (e.g., 1.8 V)
        - Step Type: Linear
        - Number of Steps/Points: Sufficiently high (e.g., 100-200 points) to get a smooth curve.
    - Specify output to be plotted: Vout.
5. **Run Simulation:** Execute the DC sweep simulation.
6. **Plot VTC:** Observe the Vout vs. Vin characteristic curve on the waveform viewer.
7. **Extract Initial VTC Parameters:** Using cursor tools or measurement functions within your simulator:
    - Determine VOH and VOL.
    - Find Vth (where Vout = Vin).
    - Locate VIL and VIH (where dVout/dVin = -1). *Refer to your simulator's manual for precise methods to find slope = -1 points.*
8. **Calculate Initial Noise Margins:**
    - NML = VIL - VOL
    - NMH = VOH - VIH

Part B: Impact of W/L Ratio on VTC and Noise Margins

1. **Varying nMOSFET W/L:**

    - Return to the schematic. Keep the pMOSFET W/L constant (e.g., W=2µm, L=0.18µm).
    - Change the nMOSFET width (W_n) to the following values (e.g.):
        - Case 1: W_n = 0.5 µm (nMOS weaker)
        - Case 2: W_n = 1.5 µm (nMOS stronger)
    - For each case, repeat steps 4-8 from Part A: Run DC sweep, plot VTC, extract VTC parameters, and calculate noise margins.
    - Record all results.
2. **Varying pMOSFET W/L:**
    - Return to the schematic. Set the nMOSFET W/L back to its initial value (W=1µm, L=0.18µm).
    - Change the pMOSFET width (W_p) to the following values (e.g.):
        - Case 1: W_p = 1 µm (pMOS weaker)
        - Case 2: W_p = 3 µm (pMOS stronger)
    - For each case, repeat steps 4-8 from Part A: Run DC sweep, plot VTC, extract VTC parameters, and calculate noise margins.
    - Record all results.
3. **Optimal Sizing (Optional/Advanced):**
    - Based on your observations, try to find an "optimal" (W/L)pMOS / (W/L)nMOS ratio that yields a Vth close to VDD/2 and provides balanced noise margins. This may involve iterating a few times.
    - Perform a DC sweep for this "optimal" design and record its parameters.

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5. Observation/Results:

Record all your measurements and calculated values in a clear, organized table format. Include columns for:

Design Case	W_n (µm)	W_p (µm)	VOH (V)	VOL (V)	Vth (V)	VIL (V)	VIH (V)	NML (V)	NMH (V)
Initial	1	2							
nMOS Weaker	0.5	2							
nMOS Stronger	1.5	2							

pMOS Weaker	1	1							
pMOS Stronger	1	3							
Optimal (if done)									

Also, include screenshots of the VTC plots for at least the initial design and one or two cases where W/L ratios were significantly varied, clearly showing the parameter extraction points (VIL, VIH, Vth). Label axes clearly.

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6. Analysis and Discussion:

Write a comprehensive analysis of your experimental results.

1. **Initial Inverter Performance:** Discuss the VTC, VTC parameters, and noise margins obtained from your initial inverter design. Are they close to ideal values? Explain any deviations.
2. **Impact of nMOSFET W/L Variation:**
    - Describe how changing the nMOSFET's W/L ratio affected the VTC curve (e.g., horizontal shift, slope changes).
    - Specifically, explain the observed changes in Vth, VIL, VIH, VOH, and VOL.
    - Discuss the resulting impact on NML and NMH. Why did these noise margins change as they did? Relate it to the relative strengths of the nMOS and pMOS transistors.
3. **Impact of pMOSFET W/L Variation:**
    - Describe how changing the pMOSFET's W/L ratio affected the VTC curve.
    - Explain the observed changes in Vth, VIL, VIH, VOH, and VOL.
    - Discuss the resulting impact on NML and NMH. How do these changes compare to varying the nMOSFET?
4. **Achieving Symmetrical VTC and Balanced Noise Margins:**
    - Based on your experiments, explain the relationship between the (W/L)pMOS / (W/L)nMOS ratio and the inverter's Vth.
    - Discuss the importance of achieving a symmetrical VTC (Vth ~ VDD/2) and balanced noise margins for robust digital circuit design.
    - If you performed the optimal sizing, describe the process you followed and the rationale behind your final chosen W/L ratios.
5. **Sources of Non-ideality:** Discuss any observed non-idealities in your VTC (e.g., VOH not exactly VDD, VOL not exactly 0V) and explain their physical reasons (e.g., channel length modulation, body effect, finite transistor output resistance).

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7. Post-lab Questions:

Answer these questions after completing the lab and analyzing your results.

1. If you have an inverter with NML = 0.4V and NMH = 0.2V, which type of noise (positive-going on logic low or negative-going on logic high) is the circuit more susceptible to? Justify your answer.
2. How would the VTC of an inverter change if VDD were increased? Assume transistor parameters remain constant.
3. Consider a scenario where the threshold voltage (Vt) of the nMOSFET unexpectedly increases significantly due to a fabrication variation. How would this affect the VTC and noise margins of a standard CMOS inverter?
4. Why is static power consumption ideally zero in a CMOS inverter when it is in a stable logic state (input at 0V or VDD)? Under what conditions would static power consumption become non-zero?
5. Discuss the trade-off between achieving a perfectly symmetrical VTC (Vth = VDD/2) and minimizing the overall footprint (area) of the inverter. When might one be prioritized over the other?